

ABSTRACT

A method of verifying a digital hardware design simulated in a hardware design language (HDL). States to be verified are defined, including signal values for each component within the hardware design. A test is applied to the hardware design, such that traces of internal signals within the hardware design are recorded. Each trace includes signal data, time data and at least the internal signals associated with the components. The traces are processed to ascertain whether the plurality of components simultaneously had the signal values associated with the state, thereby to ascertain whether the state was achieved.

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